What is claimed is:

1. A processor which decodes and executes an instruction sequence, the processor comprising:

a state hold means for holding, when a predetermined instruction is executed, a renewal state for an execution result of the predetermined instruction;

an obtaining means for obtaining an instruction sequence composed of instructions matching instructions assigned to an instruction set of the processor,

wherein the instruction set is assigned first conditional instructions, a first state condition for a first conditional instruction being mutually exclusive with a second state condition for a second conditional instruction which has a same operation code as the first conditional instruction, the instruction set not being assigned the second conditional instruction, and the first state condition and the second state condition specifying either of one state and a plurality of states;

a decoding means for decoding each instruction in the obtained instruction sequence one by one;

a judging means for judging whether the renewal state is included in either of the state and the plurality of states specified by the first state condition in the first conditional instruction, when the decoding means decodes

the first conditional instruction; and

an execution means for executing, only if a judgement result by the judging means is affirmative, an operation specified by the operation code in the first conditional instruction decoded by the decoding means.

2. The processor of Claim 1,

wherein the renewal state shows a relation between magnitudes of two comparison objects a and b, the relation corresponding to an execution result of a type of comparison instruction,

wherein execution of a first conditional instruction is only possible after a comparison instruction, and the instruction set is assigned three types of first conditional instructions, the first condition states of the three types of first conditional instructions being:

1. one out of "a=b" and "a≠b";
2. one out of "a≥b" and "a<b"; and
3. one out of "a≤b" and "a>b".

3. The processor of Claim 2,

wherein an operation code included in a conditional instruction is one of a transfer operation code, an arithmetic operation code, and a logic operation code.

4. A processor which decodes and executes an instruction sequence, the processor including:

an obtaining means for obtaining an instruction sequence composed of instructions matching instructions assigned to an instruction set of the processor,

wherein the instruction set is assigned at least one first conditional flag setting instruction, at least one second conditional flag setting instruction, and at least one conditional execution instruction,

each first conditional flag setting instruction including a first condition, and each second conditional flag setting instruction including a second condition, each first condition being mutually exclusive with one of the second conditions,

each conditional execution instruction including an operation code that is not included in any other conditional execution instruction in the instruction set;

a decoding means for decoding each instruction in the obtained instruction sequence one by one;

a conditional flag for holding a judgement result as to whether a predetermined condition is satisfied;

a judging means for judging, when the decoding means decodes the first conditional flag setting instruction, whether the first condition in the first conditional flag

setting instruction is satisfied and has the conditional flag hold a judgement result for the first condition and, when the decoding means decodes the second conditional flag setting instruction, judges whether the second condition in the second conditional flag setting instruction is satisfied and has the conditional flag hold a judgement result for the second condition; and

an execution means for executing, only if the decoding means decodes the conditional execution instruction and the judgement result held by the conditional flag indicates that a condition for the conditional execution instruction is satisfied, an operation specified by the operation code in the conditional execution instruction.

5. The processor of Claim 4,

wherein each of the first conditional flag setting instruction and the second conditional flag setting instruction specifies two comparison objects a and b,

wherein the instruction set is assigned three types of first conditional flag setting instructions and three types of second conditional flag setting instructions, the first conditions of the first conditional flag setting instructions being a combination of the following conditions:

1. one out of "a=b" and "a≠b";

2. one out of "a≥b" and "a<b"; and

3. one out of "a≤b" and "a>b",

the second conditions of the second conditional instructions being three mutually exclusive conditions for the three first conditions.

6. The processor of Claim 5,

wherein the instruction set is further assigned two types of first conditional flag setting instructions and two types of second conditional flag setting instructions,

the first conditions of the first conditional flag setting instructions being a combination of the following conditions:

4. one out of "a≥b" and "a<b"; and

5. one out of "a≤b" and "a>b"

(where a and b of conditions 4 and 5 are compared with signs of a and b being taken into account),

and the second conditions of the second conditional flag setting instructions being mutually exclusive with the first conditions.

7. The processor of Claim 5,

wherein an operation code included in a conditional

execution instruction is one of a transfer operation code, an arithmetic operation code, a logic operation code, and a branch operation code.

8. An instruction conversion apparatus for converting instruction sequences not including conditional instructions into instruction sequences including conditional instructions, each of the conditional instructions including a condition and an operation code and having a processor execute an operation specified by the operation code only if the condition is satisfied, the apparatus comprising:

an obtaining means for obtaining an instruction sequence which does not include conditional instructions;

an instruction sequence detection means for detecting, out of the obtained instruction sequence, a conversion target instruction sequence which transfers different transfer objects to a same storage resource depending on whether a predetermined condition is satisfied;

a judging means for judging whether an instruction set of a specialized processor is assigned a conditional instruction including a same condition as the predetermined condition; and

a conversion means for converting, when a judgement result by the judging means is affirmative, the conversion target instruction sequence into an instruction sequence including a conditional instruction including the predetermined condition and for interchanging, when the judgement result by the judging means is negative, the transfer objects of the conversion target instruction sequence and converts the conversion target instruction sequence into an instruction sequence including a conditional instruction including a condition that is mutually exclusive with the predetermined condition.

9. The apparatus of Claim 8,

wherein the instruction set of the specialized processor is assigned a conditional instruction including a condition that is mutually exclusive with a condition included in a conditional instruction judged as not assigned to the instruction set by the judging means, and

conditions included in conditional instructions for a same operation assigned to the instruction set are not mutually exclusive.

10. The apparatus of Claim 9,

wherein execution of a conditional instruction is

only possible after a comparison instruction, and

the instruction set is assigned three types of conditional instructions for each operation according to a relation between magnitudes of two comparison objects compared by the comparison instruction, the conditions of the three types of conditional instructions being:

1. one out of "a=b" and "a≠b";
2. one out of "a≥b" and "a<b"; and
3. one out of "a≤b" and "a>b".

11. The apparatus of Claim 10,

wherein each of the transfer objects is one of a numerical value, a value indicated by a different storage resource, an operation result of a numerical value and a value indicated by the different storage resource, an operation result of numerical values, and an operation result of values indicated by the different storage resource.

12. The apparatus of Claim 11,

wherein the conversion target instruction sequence consecutively includes a conditional branch instruction for branching to a next instruction but two, a transfer instruction for transferring a transfer object to a storage resource, an unconditional branch instruction for

branching to a next instruction but one, and a transfer instruction for transferring another transfer object to the storage resource.

13. An instruction conversion apparatus for converting conditional instructions included in instruction sequences, each of the conditional instructions including a condition and an operation code and having a processor execute an operation specified by the operation code only if the condition is satisfied, the apparatus comprising:

an obtaining means for obtaining an instruction sequence including conditional instructions;

a conditional instruction detection means for detecting a conditional instruction included in the obtained instruction sequence;

a first judging means for judging whether the detected conditional instruction is assigned to an instruction set of a specialized processor;

a second judging means for judging, when a judgement result by the first judging means is negative, whether the obtained instruction sequence includes a conversion target instruction sequence which transfers different transfer objects to a same storage resource depending on whether a predetermined condition of the detected conditional instruction is satisfied; and

a conversion means for interchanging, when a judgement result by the second judging means is affirmative, the transfer objects and converts the detected conditional instruction into a conditional instruction including a condition that is mutually exclusive with the predetermined condition.

14. The apparatus of Claim 13,

wherein the instruction set of the specialized processor is assigned a conditional instruction including a condition being mutually exclusive with a condition included in a conditional instruction judged as not assigned to the instruction set by the first judging means, and

conditions included in conditional instructions for a same operation assigned to the instruction set are not mutually exclusive.

15. The apparatus of Claim 14,

wherein execution of a conditional instruction is only possible after a comparison instruction, and

the instruction set is assigned three types of conditional instructions for each operation according to a relation between magnitudes of two comparison objects compared by the comparison instruction, the conditions of

the three types of conditional instructions being:

1. one out of "a=b" and "a≠b";
2. one out of "a≥b" and "a<b"; and
3. one out of "a≤b" and "a>b".

16. The apparatus of Claim 15,

wherein each of the transfer objects is one of a numerical value, a value indicated by a different storage resource, an operation result of a numerical value and a value indicated by the different storage resource, an operation result of numerical values, and an operation result of values indicated by the different storage resource.

17. The apparatus of Claim 16,

wherein the conversion target instruction sequence consecutively includes a comparison instruction for comparing two comparison objects, a transfer instruction for transferring a predetermined transfer object to a predetermined storage resource, and a conditional instruction for transferring a transfer object that differs from the predetermined transfer object to the predetermined storage resource only if a predetermined condition is satisfied.

18. The apparatus of Claim 13,

wherein the conversion means includes:

an inverse conversion means for converting, when a judgement result by the second judging means is negative, the instruction sequence including the detected conditional instruction into an instruction sequence not including the detected conditional instruction.

19. An instruction conversion apparatus for converting an instruction sequence not including a conditional flag setting instruction and a conditional execution instruction into an instruction sequence including a conditional flag setting instruction and a conditional execution instruction,

each conditional flag setting instruction including a condition, having a specialized processor judge whether the condition is satisfied, and having a conditional flag hold a judgement result as to whether the condition is satisfied,

each conditional execution instruction including an operation code and having the specialized processor execute an operation specified by the operation code only if a condition of the conditional execution instruction is satisfied,

the apparatus comprising:

an obtaining means for obtaining an instruction sequence which does not include conditional flag setting instructions and conditional execution instructions;

an instruction sequence detection means for detecting, out of the obtained instruction sequence, a conversion target instruction sequence which transfers different transfer objects to a same storage resource depending on whether a predetermined condition is satisfied; and

a conversion means for converting the conversion target instruction sequence into an instruction sequence which includes a conditional flag setting instruction including the predetermined condition and a conditional execution instruction including an operation code which specifies an operation for transferring a transfer object to the storage resource when the predetermined condition is satisfied.

20. The apparatus of Claim 19,

wherein a condition of a conditional flag setting instruction which is convertible by the conversion means is mutually exclusive with a condition of another conditional flag setting instruction which is convertible by the conversion means.

21. The apparatus of Claim 20,

wherein each conditional flag setting instruction specifies two comparison objects a and b,

wherein the instruction set is assigned three types of first conditional flag setting instructions and three types of second conditional flag setting instructions, the first conditions of the first conditional flag setting instructions being a combination of the following conditions:

1. one out of "a=b" and "a≠b";

2. one out of "a≥b" and "a<b"; and

3. one out of "a≤b" and "a>b",

the second conditions of the second conditional flag setting instructions being three mutually exclusive conditions for the three first conditions.

22. The apparatus of Claim 21,

wherein each of the transfer objects is one of a numerical value, a value indicated by a different storage resource, an operation result of a numerical value and a value indicated by the different storage resource, an operation result of numerical values, and an operation result of values indicated by the different storage resource.

23. The apparatus of Claim 22,

wherein the conversion target instruction sequence consecutively includes a comparison instruction for comparing two comparison objects, a conditional branch instruction for branching to a next instruction but two when a predetermined condition is satisfied, a transfer instruction for transferring a predetermined transfer object to a predetermined storage resource, an unconditional branch instruction for branching to a next instruction but one, and a transfer instruction for transferring a transfer object that differs from the predetermined transfer object to the predetermined storage resource.

24. The apparatus of Claim 22,

wherein the conversion target instruction sequence consecutively includes a comparison instruction for comparing two comparison objects, a transfer instruction for transferring a predetermined transfer object to a predetermined storage resource, and a conditional instruction for transferring a transfer object that differs from the predetermined transfer object to the predetermined storage resource only if a predetermined condition is satisfied.

25. The apparatus of Claim 22,

wherein the conversion target instruction sequence consecutively includes a comparison instruction for comparing two comparison objects, a conditional instruction for transferring a predetermined transfer object to a predetermined storage resource only if a predetermined condition is not satisfied, and a conditional instruction for transferring a transfer object that differs from the predetermined transfer object to the predetermined storage resource only if the predetermined condition is satisfied.

26. A computer-readable recording medium which records an instruction conversion program for having a computer perform a method of converting instruction sequences not including conditional instructions into instruction sequences including conditional instructions, each of the conditional instructions including a condition and an operation code and having a processor execute an operation specified by the operation code only if the condition is satisfied, the program comprising:

an obtaining step for obtaining an instruction sequence which does not include conditional instructions;

an instruction sequence detection step for detecting,

out of the obtained instruction sequence, a conversion target instruction sequence which transfers different transfer objects to a same storage resource depending on whether a predetermined condition is satisfied;

a judging step for judging whether an instruction set of a specialized processor is assigned a conditional instruction including a same condition as the predetermined condition; and

a conversion step for converting, when a judgement result in the judging step is affirmative, the conversion target instruction sequence into an instruction sequence including a conditional instruction including the predetermined condition and for interchanging, when the judgement result in the judging step is negative, the transfer objects of the conversion target instruction sequence and converts the conversion target instruction sequence into an instruction sequence including a conditional instruction including a condition that is mutually exclusive with the predetermined condition.

27. A computer-readable recording medium which records an instruction conversion program for having a computer perform a method of converting conditional instructions included in instruction sequences, each of the conditional instructions including a condition and an operation code

and having a processor execute an operation specified by the operation code only if the condition is satisfied, the program comprising:

an obtaining step for obtaining an instruction sequence including conditional instructions;

a conditional instruction detection step for detecting a conditional instruction included in the obtained instruction sequence;

a first judging step for judging whether the detected conditional instruction is assigned to an instruction set of a specialized processor;

a second judging step for judging, when a judgement result in the first judging step is negative, whether the obtained instruction sequence includes a conversion target instruction sequence which transfers different transfer objects to a same storage resource depending on whether a predetermined condition of the detected conditional instruction is satisfied; and

a conversion step for interchanging, when a judgement result in the second judging step is affirmative, the transfer objects and converts the detected conditional instruction into a conditional instruction including a condition that is mutually exclusive with the predetermined condition.

28. A computer-readable recording medium which records an instruction conversion program for having a computer perform a method of converting an instruction sequence not including a conditional flag setting instruction and a conditional execution instruction into an instruction sequence including a conditional flag setting instruction and a conditional execution instruction,

each conditional flag setting instruction including a condition, having a specialized processor judge whether the condition is satisfied, and having a conditional flag hold a judgement result as to whether the condition is satisfied,

each conditional execution instruction including an operation code and having the specialized processor execute an operation specified by the operation code only if a condition of the conditional execution instruction is satisfied,

the program comprising:

an obtaining step for obtaining an instruction sequence which does not include conditional flag setting instructions and conditional execution instructions;

an instruction sequence detection step for detecting, out of the obtained instruction sequence, a conversion target instruction sequence which transfers different transfer objects to a same storage resource depending on

whether a predetermined condition is satisfied; and

a conversion step for converting the conversion target instruction sequence into an instruction sequence which includes a conditional flag setting instruction including the predetermined condition and a conditional execution instruction including an operation code which specifies an operation for transferring a transfer object to the storage resource when the predetermined condition is satisfied.